CBCS SCHEME

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15CS72

Seventh Semester B.E. Degree Examination, Jan./Feb. 2023
Advanced Computer Architectures

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. What is Computer Architecture? Give Flynn's classification of computer architecture. **(06 Marks)**

b. A 400MHz processor was used to execute a benchmark program with the following instruction mix and clock cycle count:

Instruction type	Instruction count	Clock cycle count
Integer arithmetic	450000	1
Data transfer	320000	2
Floating point	150000	2
Control transfer	80000	2

Determine the effective CPI, MIPS rate and execution time for this program. **(04 Marks)**

c. With a neat diagram, explain the operational model of SIMD computers. **(06 Marks)**

OR

2 a. Explain how digital bus and cross bar network can be used as dynamic interconnection networks. **(10 Marks)**

b. State Amdahl's law. Define system efficiency, redundancy, utilization and quality of parallelism. **(06 Marks)**

Module-2

3 a. Compare the Architectural design and various parameters in RISC and CISC processors. **(05 Marks)**

b. Explain the use of translation Look aside Buffer (TLB) and page tables for address mapping. **(06 Marks)**

c. Explain the inclusion property and data transfer between adjacent levels of memory hierarchy with an example. **(05 Marks)**

OR

4 a. With a neat diagram, explain the architecture of a Very Long Instruction Word (VLIW) processor and its pipeline operations. **(10 Marks)**

b. Explain the memory page replacement policies. **(06 Marks)**

Module-3

5 a. What is an arbitration? Explain the three arbitration schemes. **(08 Marks)**

b. Explain the following block placement schemes:
i) Direct mapping
ii) Set associative caches. **(08 Marks)**

OR

6 a. Explain the Branch Handling techniques. **(08 Marks)**

b. With a neat diagram, explain the design of a pipelined floating point unit built as on chip features in Motorola M68040 processor. **(08 Marks)**

Module-4

7 a. What is Snoopy bus protocol? Explain write through, write back and write-once cache protocol. **(08 Marks)**

b. Explain the different types of message routing schemes. **(08 Marks)**

OR

8 a. Define vector processor. Explain different vector instruction types by mathematical mappings between their working register or memory where vector operands are stored. **(08 Marks)**

b. Explain multithreaded architecture and its computation model for a massively parallel processing system. **(08 Marks)**

Module-5

9 a. Explain the compilation phases in parallel code generation. **(08 Marks)**

b. Explain the principle of synchronization. **(08 Marks)**

OR

10 a. Explain the processor design with reorder buffer. **(06 Marks)**

b. What is Data Dependences? Explain the different types of data dependence. **(07 Marks)**

c. Write the state transition diagram of 2-bit branch predictor. **(03 Marks)**

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